Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (Cancelled)

11. (Currently Amended) ~~A semiconductor~~ An integrated circuit structure formed on a substrate, comprising:

a first dielectric layer comprising a plurality of fluorinated carbon nanostructures and a copolymer layer binding said fluorinated carbon nanostructures; [[and]]

an opening with a sidewall extending into said first dielectric layer;

~~at least one~~ a conductive feature disposed in said opening in said first dielectric layer, said ~~at least one~~ conductive feature electrically isolated from nearby conductive features by portions of said first dielectric layer; and

a second dielectric layer disposed in said opening between said conductive feature and said first dielectric layer, said second dielectric layer comprising a dielectric material that prevents migration of conductive material from said conductive feature through said sidewall and into said first dielectric layer.

12. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 wherein said first dielectric layer has an exposed surface, and further comprising: a cap layer ~~of an insulating material~~ at least partially covering said exposed surface, said cap layer having a top surface, and said conductive feature having a top surface substantially coplanar with said top surface of said cap layer.

13. (Cancelled)

14. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 wherein said fluorinated carbon nanostructures comprise a plurality of fluorinated carbon nanotubes.

15. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 wherein said first dielectric layer has a dielectric constant of less than about 3.

16. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 wherein said structure comprises a plurality of ~~conductors~~ conductive features electrically isolated by portions of said dielectric layer ~~of said dielectric material~~.

17. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 wherein said fluorinated carbon nanostructures comprise a plurality of fluorinated carbon buckyballs.

18. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 further comprising:

a cap layer disposed on said ~~fluorinated carbon nanostructures~~ first dielectric layer.

19. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 18 wherein said fluorinated carbon nanostructures, said copolymer layer, and said cap layer collectively have a dielectric constant of less than about 3.

20. (Currently Amended) The ~~semiconductor~~ integrated circuit structure of claim 11 further comprising:

a substrate selected from the group consisting of an interconnect level, a dielectric material, a buried barrier layer, a metallization line, and a semiconductor wafer.

21. (Currently Amended) An integrated circuit comprising a plurality of circuit elements and the ~~semiconductor~~ integrated circuit structure of claim 11, said ~~at least one~~ conductive feature being electrically coupled with at least one of said circuit elements.

22. (Cancelled)

23. (Currently Amended) The ~~dielectric material~~ integrated circuit structure of claim 11 wherein said fluorinated carbon nanostructures and said copolymer layer have an effective dielectric constant of less than about 3.

24-45. (Cancelled)

46. (New) The integrated circuit structure of claim 11 further comprising:

a plurality of mandrels in said first dielectric layer, each of said mandrels including sidewalls from which said fluorinated carbon nanostructures project into said copolymer layer.

47. (New) The integrated circuit structure of claim 11 further comprising:

a catalyst layer bordering said first dielectric layer, said catalyst layer comprising a metal-containing material capable of promoting synthesis of said fluorinated carbon nanostructures.

48. (New) The integrated circuit structure of claim 11 further comprising:

a liner layer of a conductive material disposed between said second dielectric layer and said conductive feature.